An Active Millimeter Wave MMIC Frequency Doubler with High Spectral Purity and Low Power Consumption

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Abstract — **The design and characterization of a millimeterwave frequency doubler based on a commercial foundry HEMT-process is described. The main goal of this work was to create a doubler topology which is simple, reliable, electrically stable and in addition has low power dissipation, good spectral purity, and high bandwidth. The presented doubler is based on an input stage biased close to pinch-off for efficient harmonic generation, followed by a frequency selective amplifier. The doubler chip occupies about 2 mm^2 chip area and delivers 7 dBm output power with an excellent rejection of unwanted harmonics of >34dB and a DC-power consumption of only 40 mW. The 3 dB bandwidth is 25%.**

I. Introduction

Frequency multipliers are quite common in microwave and millimeter wave systems like radio links and radars. Reasons for using frequency doublers are the lack of fundamental frequency oscillators with sufficiently good phase noise performance or simply lack of existing oscillators at millimeter wave frequencies. Frequency multipliers are quite well described in the literature. Frequency multiplication can be achieved by resistive or varactor multiplication by using diodes, step recovery based multipliers, Maas [1], or passive, Jonsson et al [2] and active multipliers using transistors, Rausher [3] and Arai et al [4]. Active multipliers are perhaps the most popular type today due to the possibility of conversion gain and availability of good FET or HEMT devices. MMIC-based active frequency multipliers have been realized and reported in the literature, Kawasaki et al [5], they can be made 'single ended' or balanced depending on the required rejection of unwanted harmonics. This is important in certain communication applications like phase modulation. Typical rejection requirements are 40 dBc. Balanced operation is normally obtained by utilizing an input balun, Angelov et al [6], but can also be obtained with a common-source common-gate configuration, Hiraoka et al [7]. Since the balanced multiplier can offer excellent rejection over a broad bandwidth it is often chosen, but on the other hand the power dissipation and the chip size (and consequently also the prize) is normally also more than doubled. Therefore there is a need for a simple small sized topology which can fulfil all the above mentioned goals. We will show that a single ended active HEMT frequency doubler is a good alternative in achieving all goals at the same time. We will also describe the fundamental design steps for this kind of doubler.

II. Doubler Design

The circuit topology for the doubler is shown in Fig. 1. The frequency doubler consists of two active cascaded HEMT-stages, the first is biased close to pinch-off in order to generate a drain current which is rich of harmonics, the second transistor is amplifying the second harmonic of the input signal. The gatewidth of the transistors are 100 μm in this design.

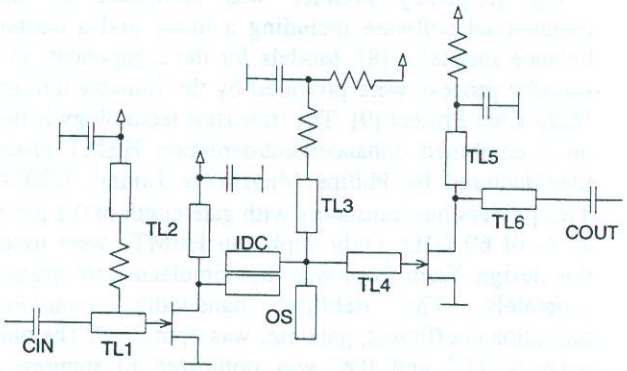

Fig. 1: Schematic of the frequency doubler.

The drain of the first HEMT is biased through a transmission line, TL2, which is RF-shorted at its end by a capacitor connected to a via-short. In order to reject the fundamental frequency, TL2 has a short electrical length at the fundamental frequency, ideally the drain should be shorted at the fundamental frequency. On the other hand TL2 has to be long enough at the second harmonic so that second harmonic power can be delivered to the second stage. The second stage should amplify the frequency band of the second harmonic and reject other frequencies i. e. have a band pass characteristic. To achieve rejection of the fundamental frequency, an inter digital capacitor (IDC) is used with an electrical length shorter than $\lambda/4$.

The open stub (OS) is used for impedance matching. Also the output stage has an electrically short transmission line, TL5, as part of the output matching network in order to suppress the gain at the fundamental frequency. The stability of the design was achieved by checking the stability factor for unconditionally stability for all frequencies and bias points, stability was achieved by placing stabilizing resistors at the input of stage 1, in the interstage network, and at the output. The gate bias and drain bias for both devices can be controlled independently in order to allow for the investigation of bias sensitivity. The input and output are galvanically isolated from the circuit through coupling capacitors. The chip size is 1×3 mm (since this is the closest available size in the multi project wafer) which can be easily compressed to below 2 mm^2. A photo of the chip is shown Fig. 2 below.

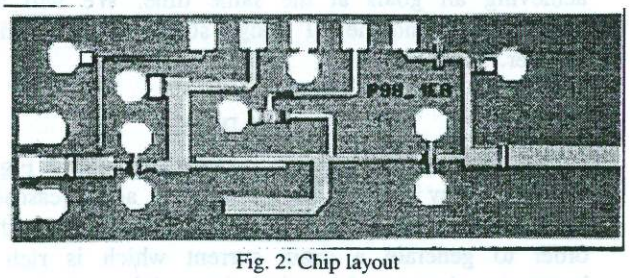

Fig. 2: Chip layout

III. Simulation Results

The frequency doubler was simulated by using commercial software including a linear and a harmonic balance simulator [8]. Models for the components in the foundry process were provided by the foundry through a Multi Chip Project [9]. The transistor technology is based on a combined enhancement/depletion HEMT process, manufactured by Philips Microwave Limeil, ED02AH. This process has transistors with gatelength of 0.2 μm and an f_T of 60 GHz. Only depletion HEMTs were used in this design. Each stage was first simulated and optimized separately. The stability, bandwidth, input/output reflection coefficient, gain etc. was optimized. The output network TL2 and IDC was optimized to suppress the fundamental frequency. The first stage was then simulated by using a harmonic balance simulator, the harmonic content at the output was investigated as a function of gate and drain bias voltage, and input power. The optimum gate-bias voltage was then chosen for maximum second harmonic generation. After optimization of the output stage, both stages were connected and the complete circuit was then simulated and optimized. Some simulation results are especially interesting like the input/output power characteristics, current and voltage-waveforms at the gate and drain of the first transistor, and the bandwidth analysis. Some of the results are shown in Fig. 3, 4, 5, and 6. From Fig. 3 we conclude that a maximum output power of 6 dBm can be achieved at an input power of 8-10 dBm. The suppression of all unwanted harmonics is better that 20 dBc and is improved with increasing output power for the fundamental case. The dissipated dc power is 30 mW at low signal levels and is increasing to approximately 70 mW at full output power. The drain current waveform is approximately 'cosine-pulse' i.e. similar to half wave rectified sinus at low input levels. In the compression region the waveform is more rectangular due to the fact that the drain-current is saturated at high gate voltage. This is illustrated in Fig. 4 where the drain-current is plotted at an input power of 5 and 10 dBm respectively. This behavior is more pronounced for a HEMT compared to the MESFET because the drain-current versus gate-voltage characteristic of a HEMT is efficiently saturated at high gate voltage.

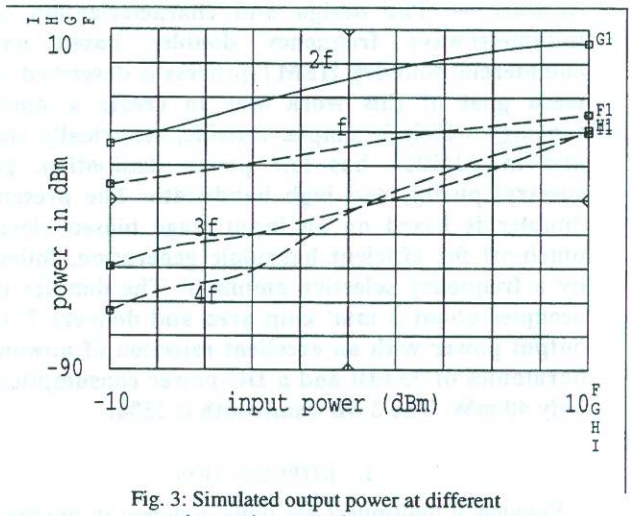

Fig. 3: Simulated output power at different harmonics versus input power

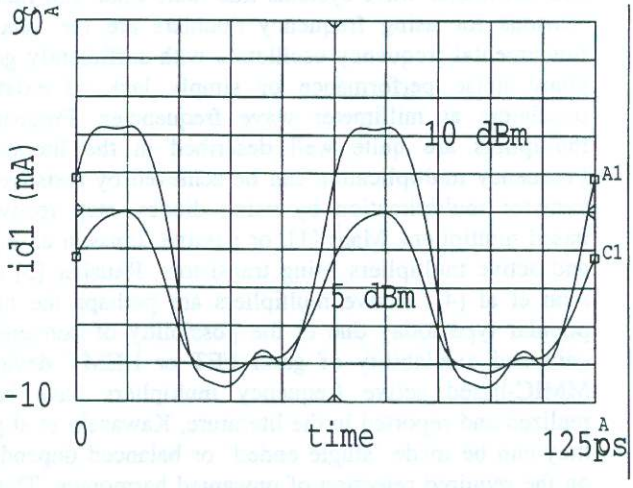

Fig. 4: The drain current waveform at 5 and 10 dBm

At an input power of 10 dBm, the capacitive current through Cgs can be substantial, this is shown in Fig 5, where the dc and fundamental component of the gate-current is plotted versus the input power. The dc-current is due to rectification in the gate Schottky junction, this current is 200 μA at 10 dBm input power while the amplitude of the fundamental component is 13 mA! It is for the moment not clear if this will have any impact of

the long-term reliability, it is however possible to decrease this current by for instance including a resistor in series with the gate.

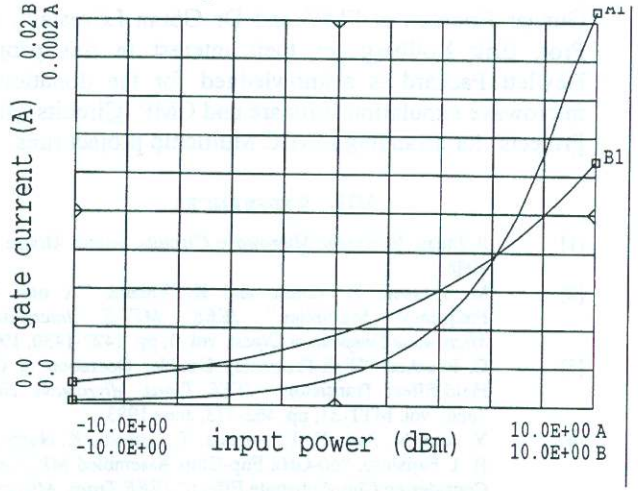

Fig. 5: Gate current at DC and fundamental versus input power, A1 is the dc-current and B1 the current at the fundamental frequency

The frequency dependence of the output power was also investigated. The fundamental power is plotted in Fig 6 for an input power of 0, 5, and 10 dBm versus input frequency. The output power is maximum at 14.5 GHz and the response is flatter at higher input power. The 3 dB bandwidth at 10 dBm input power is 10 GHz referred to the output frequency, i.e. more than 30%.

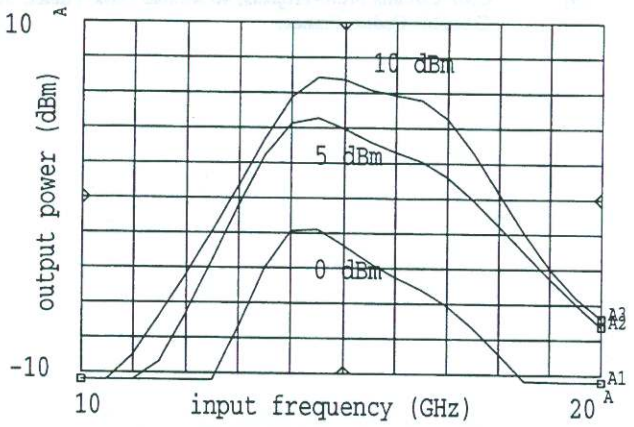

Fig. 6: Frequency dependence of the output power

IV. Experimental Results

The experimental verification has been performed using on-chip power measurements utilizing coplanar probing techniques. The output power was measured by using a HP 83650A generator, a HP 8565E spectrum analyzer, and a HP 8757 scalar network analyzer. A HP 8349B amplifier was also used in order to get sufficient input power. Attenuation in cables and probes were measured and corrected for.

The MMIC was measured at a bias condition of Vds=2 V, and Vgs=-0.6 V. At an input power of P_{in}=5 dBm, the output power was 6 dBm. The DC-power dissipation under these conditions was 40 mW. The efficiency is 9% if we define it as the ratio between output power and the total input power (i. e. including the DC-power).

The measured output power for the different harmonics versus input power at 16 GHz is plotted in fig.7.

From Fig. 8, where the frequency response is plotted, a 3 dB bandwidth of 25% is observed.

Derived from the measurement illustrated in Fig. 7 are the results shown in Fig. 9. Suppression of unwanted harmonics by more than 34 dB is obtained.

Fig. 10 shows the suppression of unwanted harmonics versus gate voltage. This figure shows that the gate bias condition chosen for the measurements is optimal in terms of harmonic suppression.

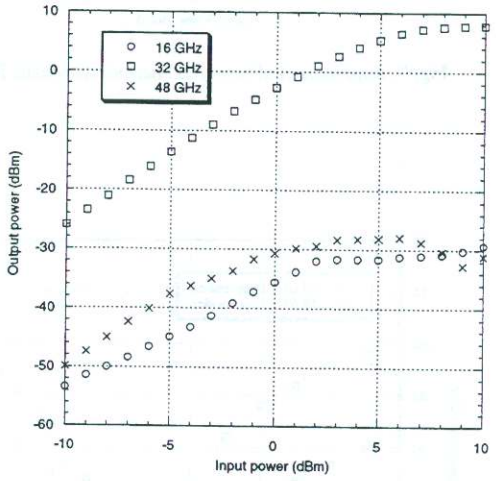

Fig. 7: Output power at different harmonics versus input power

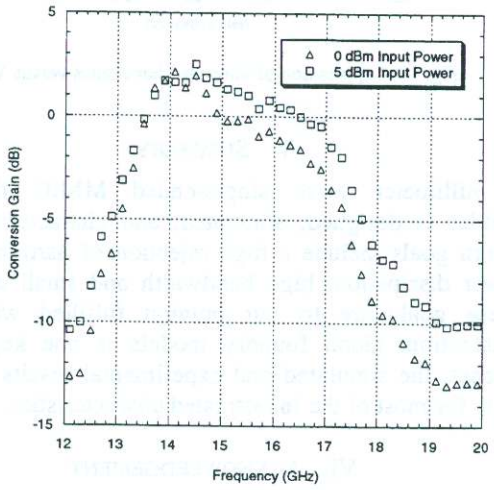

Fig. 8: Frequency response

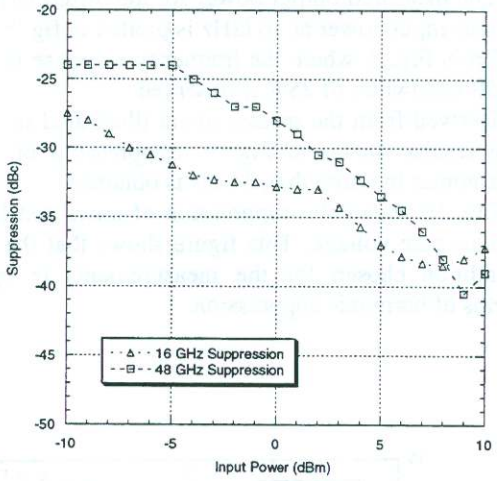

Fig. 9: Suppression of unwanted harmonics versus Pin

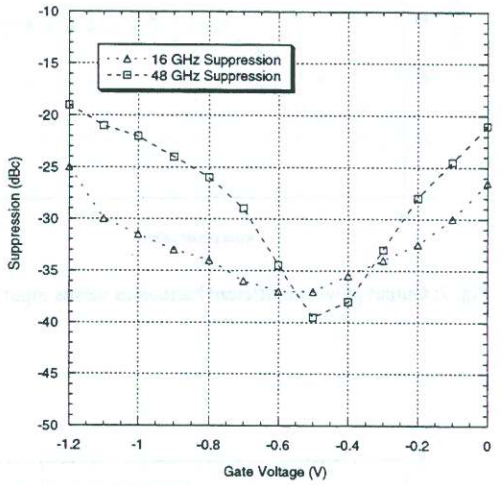

Fig. 10: Suppression of unwanted harmonics versus Vgs

V. Summary

A millimeter wave single-ended MMIC frequency doubler is designed, simulated, and characterized. The design goals include a high rejection of harmonics, low power dissipation, high bandwidth and small chip size. These goals are to our opinion fulfilled with great satisfaction. Good foundry models is one key of the success, the simulated and experimental results are very close for most of the investigated characteristics.

VI. Acknowledgement

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VII. References

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